L Number	Hits	Search Text	DB	Time stamp
1	13982	para$5 adj1 capacitance$1	USPAT; US-PGPUB	2001/12/07 14:51
4	58831	439/$.ccls.	USPAT; US-PGPUB	2001/12/07 14:52
7	39	(para$5 adj1 capacitance$1) and 439/$.ccls.	USPAT; US-PGPUB	2001/12/07 14:54
10	12432	parasitic adj1 capacitance$1	USPAT; US-PGPUB	2001/12/07 14:54
13	34	439/$.ccls. and (parasitic adj1 capacitance$1)	USPAT; US-PGPUB	2001/12/07 14:54

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PGPUB-DOCUMENT-NUMBER: 20010021608
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010021608 A1

TITLE: Crosstalk reducing electrical jack and plug connector

PUBLICATION-DATE: September 13, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Borbolla, Ian Rubin de la	Memphis	TN	US	
	Cordova	TN	US	
Hammond, Bernard	West Hempstead	NY	US	
Bennett, Anthony E.	Syosset	NY	US	
Sack, Alan M.				

US-CL-CURRENT: **439/676**

ABSTRACT:

An electrical jack and plug connector each reducing crosstalk between signal wires pairs connected to the jack and plug connectors. The jack connector including a plurality of signal carrying elements and a printed circuit board placed adjacent to the signal carrying elements. The printed circuit board includes conductive traces extending from the signal carrying elements. The conductive traces are spaced from each other to form capacitive coupling between the traces and the signal carrying elements. The signal carrying element may include both conductive contacts and conductive paths formed on the
printed circuit board. The conductive paths are routed such that capacitive and inductive coupling occurs between signal pair whereby crosstalk is reduced.
The plug connector is selectively insertable in the jack and includes a housing
in which signal wires may be inserted. Within the plug, the signal wires are routed such that a wire from signal pair cross wires of other signal pairs such
that crosstalk is reduced. Both the jack and plug connectors permit the signal
pair to remain together upon entering the connector and the signals are rerouted such that the signal at the outputs of the connectors are sequentially
arranged for compatibility purposes.

CCPR:
439/676

DETX:
[0077] Desirable amounts of capacitive coupling may be achieved by using a set of conductive traces 52 which end in tabs 54 formed on opposite sides of PCB 28
which acts as a dielectric. The induced capacitance also assists in countering
the **parasitic capacitance** which occurs between the adjacently disposed conductive plates held within plug 12.

US 20010021608A1

(19) United States

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Borbolla et al. (43) Pub. Date: Sep. 13, 2001

(54) CROSSTALK REDUCING ELECTRICAL JACK AND PLUG CONNECTOR

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(21) Appl. No.: 09/842,328

(22) Filed: Apr. 25, 2001

Related U.S. Application Data

(63) Continuation of application No. 09/293,308, filed on Apr. 16, 1999, now Pat. No. 6,231,397, which is a non-provisional of provisional application No. 60/081,985, filed on Apr. 16, 1998 and which is a non-provisional of provisional application No. 60/089,477, filed on Jun. 16, 1998 and which is a non-provisional of provisional application No. 60/127,492, filed on Apr. 2, 1999.

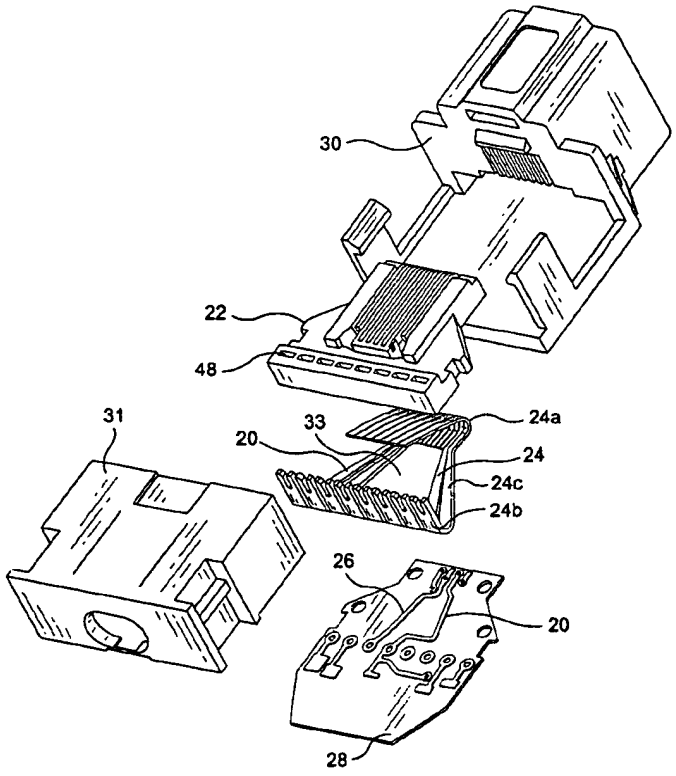
Publication Classification

(51) Int. Cl.[7] H01R 24/00

(52) U.S. Cl. 439/676

(57) ABSTRACT

An electrical jack and plug connector each reducing crosstalk between signal wires pairs connected to the jack and plug connectors. The jack connector including a plurality of signal carrying elements and a printed circuit board placed adjacent to the signal carrying elements. The printed circuit board includes conductive traces extending from the signal carrying elements. The conductive traces are spaced from each other to form capacitive coupling between the traces and the signal carrying elements. The signal carrying element may include both conductive contacts and conductive paths formed on the printed circuit board. The conductive paths are routed such that capacitive and inductive coupling occurs between signal pair whereby crosstalk is reduced. The plug connector is selectively insertable in the jack and includes a housing in which signal wires may be inserted. Within the plug, the signal wires are routed such that a wire from signal pair cross wires of other signal pairs such that crosstalk is reduced. Both the jack and plug connectors permit the signal pair to remain together upon entering the connector and the signals are rerouted such that the signal at the outputs of the connectors are sequentially arranged for compatibility purposes.



US-CL-CURRENT: 324/754

US-PAT-NO: 6325662
DOCUMENT-IDENTIFIER: US 6325662 B1
TITLE: Apparatus for testing IC chips using a sliding springy mechanism which exerts a nearly constant force apparatus
DATE-ISSUED: December 4, 2001
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tustaniwskyj; Jerry Ihor	Mission Viejo	CA	N/A	N/A

US-CL-CURRENT: **439/482**,324/754
ABSTRACT:

An electromechanical apparatus for testing IC-chips 12c includes a sliding springy mechanism 15a-15g which squeezes a chip holding subassembly 12a-12d between a temperature regulating subassembly 14a-14d and a power converter subassembly 13a-13c. Vertically moveable actuators 16a, with slots 16a-1, impart motion to joints 15e within the sliding springy mechanism 15a-15g. The joints 15e slide on a rail 15a to thereby open and close arms 15a, 15b; and that causes the substrates 14c, 12c to be lowered and raised, respectively. When the substrates 14c, 12c are raised, temperature regulating components 12c engage IC-chips 12c, and electrical contacts 12d engage electrical contacts 13b, with a force that is nearly constant despite the presence of several dimensional tolerances.

12 Claims, 26 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 18

BSPR:

Also, another drawback with the above prior art chip testing apparatus is that due to the row/column arrangement of the printed circuit boards, a large distance inherently exists between the chips that are tested and the power supplies for those chips. Due to those large distances, parasitic resistances,
parasitic inductances and **parasitic capacitances** are inherently large; and thus, the more difficult it becomes to keep the chip voltages constant while chip power dissipation changes rapidly as the chips are tested.

CCOR:
439/482

US-CL-CURRENT: **439/941**

US-PAT-NO: 6231397
DOCUMENT-IDENTIFIER: US 6231397 B1
TITLE: Crosstalk reducing electrical jack and plug connector
DATE-ISSUED: May 15, 2001
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
de la Borbolla; Ian	Memphis	TN	N/A	N/A
Rubin	Cordova	TN	N/A	N/A
Hammond; Bernard	West Hempstead	NY	N/A	N/A
Bennett; Anthony E.	Syosset	NY	N/A	N/A
Sack; Alan M.				

US-CL-CURRENT: **439/676**, **439/941**

ABSTRACT:
An electrical jack and plug connector each reducing crosstalk between signal wires pairs connected to the jack and plug connectors. The jack connector including a plurality of signal carrying elements and a printed circuit board placed adjacent to the signal carrying elements. The printed circuit board includes conductive traces extending from the signal carrying elements. The conductive traces are spaced from each other to form capacitive coupling between the traces and the signal carrying elements. The signal carrying element may include both conductive contacts and conductive paths formed on the printed circuit board. The conductive paths are routed such that capacitive and inductive coupling occurs between signal pair whereby crosstalk is reduced.
The plug connector is selectively insertable in the jack and includes a housing in which signal wires may be inserted. Within the plug, the signal wires are routed such that a wire from signal pair cross wires of other signal pairs such that crosstalk is reduced. Both the jack and plug connectors permit the signal pair to remain together upon entering the connector and the signals are rerouted such that the signal at the outputs of the connectors are sequentially arranged for compatibility purposes.
23 Claims, 32 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 30

DEPR:
Desirable amounts of capacitive coupling may be achieved by using a set of conductive traces 52 which end in tabs 54 formed on opposite sides of PCB 28 which acts as a dielectric. The induced capacitance also assists in countering the **parasitic capacitance** which occurs between the adjacently disposed conductive plates held within plug 12.

CCOR:
439/676

CCXR:
439/941

US-CL-CURRENT: 361/736,361/788 ,361/790 ,361/803 ,361/809 ,**439/61**

US-PAT-NO: 6128201
DOCUMENT-IDENTIFIER: US 6128201 A
TITLE: Three dimensional mounting assembly for integrated circuits
DATE-ISSUED: October 3, 2000
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Brown; Sammy K.	Los Gatos	CA	N/A	N/A
Avery; George E.	Saratoga	CA	N/A	N/A
Wiggin; Andrew K.	San Carlos	CA	N/A	N/A
Todd; Tom L.	San Jose	CA	N/A	N/A
Beal; Sam	Mountain View	CA	N/A	N/A

US-CL-CURRENT: 361/784,361/736 ,361/788 ,361/790 ,361/803 ,361/809 ,**439/61**
ABSTRACT:

A system and method for efficiently interconnecting a plurality of ICs, thereby improving the electrical performance of the overall system. In one embodiment of the system of the present invention, a plurality of carriers corresponds to a plurality of ICs, and a board has a plurality of board regions
for receiving the plurality of ICs and are arranged so as to be attached to a backplane forming a vertical stack of boards.
19 Claims, 15 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 11

DEPR:
Referring to FIG. 11, in another embodiment, cantilevering of the board 814 about the joints 837 may be avoided by providing a second backplane 811b, which
may be disposed opposite to the first backplane 811a or extend transversely thereto. The second backplane 811b is similar to the first backplane, but the board 814 would include first and second sets of tenons 827a and 827b, each of which is to be uniquely associated with one of the first and second back planes
811a and 811b. An added benefit of having multiple backplanes is that shorter signal paths may be provided, thereby reducing the worst case path length between signals on any boards to the average of board width plus the backplane separation. This reduces **parasitic capacitances** and inductances while increasing the transmission speed of signal in the 3-D module.

CCXR:
439/61

US-CL-CURRENT: 361/229,361/733 ,361/803 ,**439/61** ,**439/65**

US-PAT-NO: 6081430
DOCUMENT-IDENTIFIER: US 6081430 A
TITLE: High-speed backplane
DATE-ISSUED: June 27, 2000
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
La Rue; George Sterling	Bellevue	WA	98007	N/A

US-CL-CURRENT: 361/788,361/229 ,361/733 ,361/803 ,**439/61** ,**439/65**

ABSTRACT:
A backplane consisting of segmented bus lines on a mother board with loop-through connections to active transceivers mounted on connectors to daughter boards. The transceivers isolate the interconnect to the daughter boards from the bus lines. The loop-through transmission line on the connectors preserves the impedance of the bus lines and allows the interconnect
stub to the transceivers to be short, minimizing reflections and enabling high-speed backplane operation. The connectors are removable from the motherboard for repair.
6 Claims, 10 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 10

CLPR:
2. The connector of claim 1 wherein said loop-through paths are of varying widths to compensate for **parasitic capacitances** and inductances associated with
the transceiver and the connection of the transceiver to the loop-through paths.

CCXR:
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CCXR:
439/65

US-CL-CURRENT: 174/117F,174/117FF ,174/260 ,257/734 ,257/750 ,257/773 ,257/774 ,333/124 ,333/125 ,333/128 ,333/161 ,361/683 ,361/760 ,361/761 ,361/762 ,361/763 ,361/764 ,361/780 ,361/785 ,361/803 ,**439/61** ,**439/62** ,**439/65** ,**439/67**

US-PAT-NO: 5966293
DOCUMENT-IDENTIFIER: US 5966293 A
TITLE: Minimal length computer backplane
DATE-ISSUED: October 12, 1999
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Obermaier; Hannsjorg	Los Gatos	CA	N/A	N/A
Lee; Keunmyung	Palo Alto	CA	N/A	N/A

US-CL-CURRENT: 361/735,174/117F ,174/117FF ,174/260 ,257/734 ,257/750 ,257/773 ,257/774 ,333/124 ,333/125 ,333/128 ,333/161 ,361/683 ,361/760 ,361/761 ,361/762 ,361/763 ,361/764 ,361/780 ,361/785 ,361/803 ,**439/61** ,**439/62** ,**439/65** ,**439/67**

ABSTRACT:
An electrical interconnection structure. The electrical interconnection structure includes a mother board substrate having a plurality of layers. At least one layer includes a signal path having a characteristic impedance of Z.sub.O and a conductive ground plane. A signal via passes through each layer of the mother board substrate. The signal via electrically is connected to the
signal path. A ground via passes through each layer of the mother board substrate. The ground via is electrically connected to the conductive ground plane. The electrical interconnection structure further includes a plurality of flex circuits. Each flex circuit includes a flex signal path having a characteristic impedance of Z.sub.O and a flex ground plane. Each flex signal path is electrically connected to the signal via and each flex ground plane is electrically connected to the ground via. The connections between the flex signal path and the signal via, and between the flex ground plane and the ground via can be permanent or separable.
12 Claims, 13 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 11

BSPR:
The speed of the microprocessors and memory connected to the interconnection backplane is constantly increasing. As the speed of the circuitry increases, **parasitic capacitance** and impedance mismatches on the interconnection bus 12 begin to affect the integrity of the signals traveling on the bus from one component to another. As a result, the technology used to implement the interconnection backplane must evolve as the components connected to the backplane operate at faster speeds.

CCXR:
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CCXR:
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CCXR:
439/65

CCXR:
439/67

US-CL-CURRENT: 361/791,**439/924.1**

US-PAT-NO: 5432916
DOCUMENT-IDENTIFIER: US 5432916 A
TITLE: Precharge for non-disruptive bus live insertion
DATE-ISSUED: July 11, 1995
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hahn; Guenter	Sindelfingen	N/A	N/A	DEX
Muenzner; Klaus	Schoenaich	N/A	N/A	DEX
Pita; Frank J.	Cary	NC	N/A	N/A
Ulland; Hartmut	Altdorf	N/A	N/A	DEX
Diepenbrock; Joseph C.	Raleigh	NC	N/A	N/A
Oman; Price	Raleigh	NC	N/A	N/A
Kelley; Richard	Coral Springs	FL	N/A	N/A

US-CL-CURRENT: 710/302,361/791 ,**439/924.1**
ABSTRACT:
The invention is related to hot plugging of an electrical circuit (1) into a separate non-quiesced signal net (6) in an active system (7), such as a digital or analog bus. The inventive solution proposes the addition of a preconditioning network (4) to precondition the electrical circuit (1) to be hot plugged by partially precharging the parasitic input capacitances (C.sub.c, C.sub.e, C.sub.m) of the electrical circuit (1) before hot plugging. The precharging of the parasitic input capacitances serves to minimize transient effects on the active system (7).
6 Claims, 1 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 1

DEPR:
One embodiment of the present invention entails a design of a voltage divider circuit to precharge the **parasitic capacitance** of the signal net which is to be hot plugged. The voltage divider comprises a first impedance to a stable positive power supply voltage and a second impedance to a stable negative power supply voltage. The stable positive and negative power supply voltages can be established by making power and ground connections first during board insertion. The active signal net is connected later by using some staggered connection means. The relative delay between the two connections can be optimized for applications as needed. Powering up the electrical circuit to be hot plugged before engaging signal nets also assures that electrostatic discharge effects are safely grounded before logic nets are connected. Thereby stable power supply voltages can also be guaranteed before engagement of the signal nets. This eliminates the latch up exposure if CMOS logic is used on the inserted board, especially since nets can be precharged to the voltage desired. By connecting signal nets last, there is no need to use drivers or receivers that power on or off glitch free to maintain signal integrity. If power supply voltages are provided to the electrical circuit before signal nets are connected, the drivers or receivers of the electrical circuit Which is to

be hot plugged are already powered up when the signal nets of the electrical circuit finally are connected. This is advantageous in that a randomly floating output during powering up of the electrical circuit cannot disturb the
non-quiesced second signal net. Moreover, this is advantageous in that a correct power on reset can be applied to the electrical circuit before the connection of the signal nets is established.

DEPR:
The electrical circuit further comprises a signal net, preferably comprising a logic module 2 which is connected via a module I/O pin to the signal line. Thus, the printed circuit board has several parasitic capacitances: The **parasitic capacitance** of the connection interface C.sub.c, the **parasitic capacitance** of the printed circuit board edge wiring C.sub.e and the **parasitic capacitance** of the module and its I/O pin C.sub.m. The total board capacitive load is the sum of all the **parasitic capacitances,** since they are in parallel.

DEPR:
By partially charging the **parasitic capacitances** to the predefined voltage V.sub.n before the instant of connection of the signal line, these capacitances
are no longer short circuits to ground. By setting the voltage V.sub.n to the middle of the switching voltage region of the active system, or somewhat above or below this region, the invention minimizes insertion transient effects on the signal net of the active system. Thereby it is possible to manage the causes of the transient effects.

CCXR:
439/924.1

US-CL-CURRENT: 333/260

US-PAT-NO: 5145387
DOCUMENT-IDENTIFIER: US 5145387 A
TITLE: High-frequency multi-pin connector
DATE-ISSUED: September 8, 1992
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ichihashi; Toshihiro	Kumagaya	N/A	N/A	JPX

US-CL-CURRENT: **439/108**,333/260

ABSTRACT:
Three male pin contacts arranged in parallel in the same plane are mounted on a plug body of a connector plug so that the three male pin contacts form one signal transmission line. In a socket body of a connector socket for engagement with the connector plug there is provided a contact receiving chamber, in which three female contacts formed by plate springs are arranged in parallel in the same plane. The three female contacts form one signal transmission line. The center ones of the three male pin contacts and the three female contacts are used as signal lines and both side contacts are used as grounding lines, by which open microstrip line structures are formed. When the connector plug is fitted into the connector socket, each of the three female contacts are brought into contact, at one point, with the male pin contact corresponding thereto.
11 Claims, 10 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 5

BSPR:
To ensure high reliability of its contact, the conventional multi-pin connector employs the forked female contact 13 which makes contact with the male pin contact 22 at two points a and b or more as depicted in FIG. 2. With such a multi-pin contact structure, it is difficult to make the characteristic impedance of a signal path constant Further, since the connector plug 20 has a construction in which the male pin contacts 22 are disposed in parallel and signals are applied to such parallel male pin contacts 22, the signals interfere with each other, resulting in a crosstalk. Moreover, in the connector socket 10 the female contact 13 is forked and makes contact with the male pin contact 22 at the two points a and b, but when the former cannot contact with the latter at either one of the two points a and b by some cause, the non-contacting piece of the female contact 13 forms a parasitic inductance and a **parasitic capacitance**, which produce a resonance circuit or the like, adversely affecting the signal transmission characteristic.

BSPR:
According to another aspect of the present invention, one female contact is made to contact with each male contact of the connector plug, parasitic inductance and **parasitic capacitance** formed by the contacts are small and, consequently, even if the contact condition changes, the change in the parasitic inductance and capacitance is small, thus maintaining the characteristic impedance constant.

BSPR:
Thus, the present invention permits matching of the characteristic impedance

of
each signal transmission line to a desired impedance and prevents appreciable change in a parasitic inductance and a **parasitic capacitance**, and hence provides a high-frequency connector which is free from reflection or other undesirable phenomenon.

DEPR:
Since the connector of the present invention is constructed so that the male pin contacts of each triad of the connector plug contact at one point the female contacts of the corresponding triad of the connector socket as described
above, the **parasitic capacitance** or inductance is so small that the characteristic impedance of the transmission line can be held at a desired value.

CCOR:
439/108

US-CL-CURRENT: **439/678,439/924.1**

US-PAT-NO: 4549036
DOCUMENT-IDENTIFIER: US 4549036 A
TITLE: Circular integrated circuit package
DATE-ISSUED: October 22, 1985
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Reichbach; Morris M.	Lakewood	NJ	08701	N/A

US-CL-CURRENT: 174/52.2,**439/678** ,**439/924.1**

ABSTRACT:
A circular integrated circuit package which allows a large number of internal and external connections to be made to an integrated circuit chip by arranging the pin connections as rings of concentric circles. This arrangement
provides the highest possible packing density and minimizes parasitic inductances and capacitances. The circular geometry also provides for greater predictability of parasitic effects and propagation delays due to the circular symmetry of the packaging. Insertion into a printed circuit board is facilitated by decreasing the length of each successive ring of pins as the radial distance from the center of the concentric rings increases so that one ring of pins is inserted at a time. Internally, the length of internal pins may similarly be arranged, but in reverse order, so that lead length is minimized. A variety of keyway types is provided.
1 Claims, 5 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 1

BSPR:
As the number of gate equivalents per VLSI chip increases, the number of pins is expected to increase and, therefore the length of the package is also expected to increase. Large rectangular packages have a number of disadvantages. First, long packages contain long leads between the IC chip itself and the external circuit creating a large **parasitic capacitance** component and a large parasitic inductance component. These parasitic components are particularly troublesome in high frequency circuits where parasitic reactances approach circuit design reactances. Second, a large number of pins requires that the ratio of silicon area to packaging area increase at a drastic rate, while the most requirements are for increasing complex dense packaging. Thirdly, rectangular packages require lead placements
which introduce non-symmetrical design considerations since there is little symmetry in a rectangular configuration compared, say, to a circular or spherical configuration.

CCXR:
439/678

CCXR:
439/924.1

US-CL-CURRENT: 257/700,257/774 ,257/784 ,361/771 ,361/778 ,361/795 ,**439/72**

US-PAT-NO: 4225900
DOCUMENT-IDENTIFIER: US 4225900 A
TITLE: Integrated circuit device package interconnect means
DATE-ISSUED: September 30, 1980
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ciccio; Joseph A.	Winchester	MA	N/A	N/A
Thun; Rudolf E.	Carlisle	MA	N/A	N/A
Fardy; Harry J.	Chelmsford	MA	N/A	N/A

US-CL-CURRENT: 361/739,257/700 ,257/774 ,257/784 ,361/771 ,361/778 ,361/795 ,**439/72**

ABSTRACT:
An integrated circuit device package is disclosed wherein a pair of dielectric support structures are provided, each one having a pattern of electrical conductors for interconnecting integrated circuit devices disposed thereon. The electrical conductors have end portions terminating into a plurality of contact pads disposed on a first surface of the support structures. A first one of the pair of support structures has corresponding contact pads on a second, opposite surface of the support structure, each one of the contact pads on the first surface being electrically connected to a corresponding one of the contact pads on the second surface. A dielectric spacer having a plurality of electrical contact pins is disposed between the pair of support structures. One end of each pin is electrically connected to a corresponding one of the contact pads disposed on the second surface of the first one of such structures, and the other end of such contact pin is electrically connected to a corresponding one of the contact pins disposed on the first surface of the second one of the structures. The contact pins are relatively short and thereby provide a relatively short electrical interconnect for the integrated circuit devices, thereby reducing **parasitic capacitances** normally associated with electrical interconnects.
5 Claims, 5 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 3

ABPL:
An integrated circuit device package is disclosed wherein a pair of dielectric support structures are provided, each one having a pattern of electrical conductors for interconnecting integrated circuit devices disposed thereon. The electrical conductors have end portions terminating into a plurality of contact pads disposed on a first surface of the support structures. A first one of the pair of support structures has corresponding contact pads on a second, opposite surface of the support structure, each one of the contact pads on the first surface being electrically connected to a corresponding one of the contact pads on the second surface. A dielectric spacer having a plurality of electrical contact pins is disposed between the pair of support structures. One end of each pin is electrically connected to a corresponding one of the contact pads disposed on the second surface of the first one of such structures, and the other end of such contact pin is electrically connected to a corresponding one of the contact pins disposed on the first surface of the second one of the structures. The contact pins are relatively short and

thereby provide a relatively short electrical interconnect for the integrated circuit devices, thereby reducing **parasitic capacitances** normally associated with electrical interconnects.

BSPR:
While these packaging concepts have been found useful in many applications, it is, however, characterized by relatively large **parasitic capacitances** resulting
from relatively long interconnect wires used to interconnect the printed circuit boards. These **parasitic capacitances** may be sufficiently large to adversely affect their use in many low power, high density integrated circuits such as complementary metal-oxide-semiconductor (CMOS)/silicon on sapphire (SOS) circuits, short channel NMOS circuits and I.sup.2 L circuits which operate with relatively small input signal voltage swings and which, due to their relatively high output impedances, will be slowed down when forced to operate with **parasitic capacitances** normally associated with printed circuit board and individual wire back panel interconnects.

BSPR:
In accordance with the present invention, a pair of dielectric support structures, each one having a pattern of electrical conductors with end portions terminating into a plurality of contact pads disposed on a first surface of such support structures, is provided. A first one of the pair of support structures has corresponding contact pads on a second, opposite, surface, each one of the contact pads on the first surface being electrically connected to a corresponding one of the contact pads on the second surface. A dielectric spacer having a plurality of electrically insulated contact pins passing through it is disposed between the pair of dielectric support structures. One end of each contact pin is electrically connected to a corresponding one of the contact pads disposed on the second surface of the first one of the dielectric support structures, and the other end of such contact pin is electrically connected with a corresponding one of the contact pins disposed on the first surface of the second one of such dielectric support
structures. The contact pins are relatively short and thereby provide a relatively short electrical interconnect for the patterns of conductors, thereby reducing the **parasitic capacitance** normally associated with such electrical interconnects.

CCXR:
439/72